Linearity Enhancement Algorithms of Multi-bit ΔΣ DA Converter –DWA, Self-Calibration and Their Combination

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Abstract. This paper presents several linearity improvement algorithms for multi-bit ΔΣ digital-to-analog converters (DACs), utilizing digital signal processing (DSP) techniques. The ΔΣ DACs are used for electronic measurement and automatic test equipment as well as audio systems, for their easy implementation of high resolution and high linearity. However, their multi-bit configuration (which consists of a digital ΔΣ modulator and a multi-bit DAC) causes the DAC non-linearity due to characteristics mismatches among multiple unit cells, even though they can be implemented with small hardware and power. Therefore, we investigate several algorithms, Data-Weighted Averaging (DWA) algorithms and self-calibration as well as their combination, which improve the overall ΔΣ DAC linearity. We have simulated a ternary (three values: positive, zero, negative) DAC as well as a binary (two values: positive, zero) DAC. From these simulations, we have found that for the low-pass (LP) signal band, DWA type I is effective in case of both ternary and binary DACs; for the high-pass (HP) signal band, DWA type I is effective in the case of the ternary, whereas DWA type II is effective in the case of the binary. The proposed algorithms use DSP techniques and hence they are easy to implement.

1. Introduction

A ΔΣ DAC consists of mostly digital circuits, and it is frequently used for electronic measurement and test equipment as well as audio systems because it can produce highly linear DC and low frequency signal with high resolution. A multi-bit DAC has three merits. (i) High Signal-to Quantization Noise Ratio (SQNR) with a given oversampling ratio. (ii) Improvement of loop stability for a high order modulator. (iii) Relaxed requirements of the following analog filter [1, 2].

Notice that a single-bit DAC is inherently linear, whereas the multi-bit configuration causes overall DAC non-linearity due to characteristics mismatches among multiple unit cells, even though the multi-bit ΔΣ DAC can be implemented with small hardware and power [3-7]. Therefore, we have investigated the data weighted averaging (DWA) algorithm and digital self-calibration technique and their combination which improve the overall linearity of several-type ΔΣ DACs. Also we consider the case of ternary digital values (positive, zero, negative) [8], besides binary digital case (positive or zero). We show MATBAB simulation results for low-pass (LP) and high-pass (HP) ΔΣ DA modulators in14-bit resolution case. These are the extension of the contents presented in [9].

2. ΔΣ DA modulator

A LP ΔΣ DA modulator consists of all digital circuits with feedback configuration using an integrator and a comparator (Fig. 1). The error signal is accumulated at the integrator, and its output is compared by a comparator. The comparator output (positive or zero) is the ΔΣ modulator output. (Notice that in most actual implementation, the most significant bit (MSB) of the integrator is equivalently used as the comparator output [1, 2].) Also the comparator output is fed back to the input.

It is known in [1, 2] that the output power spectrum is noise-shaped; the quantization noise is reduced at low frequency while increased at high frequency (Fig. 2).

Similarly, Fig. 3 shows a HP ΔΣ DA modulator. Compared with the LP ΔΣ DA modulator (Fig. 1), plus and minus signs at the feedback summation are reversed. Fig. 4 shows that the output power spectrum is noise-shaped; the quantization noise is reduced in the high frequency regions, while it is increased at the low frequency regions.

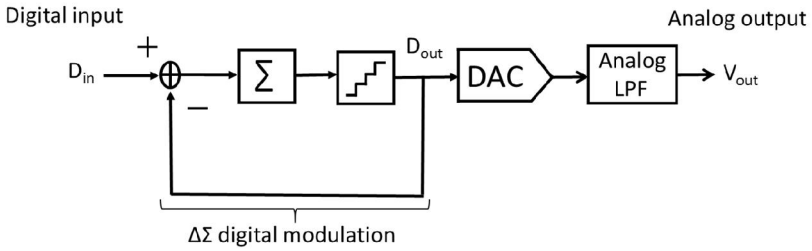


Fig. 1. Block diagram of the first-order LP ΔΣ DA converter.

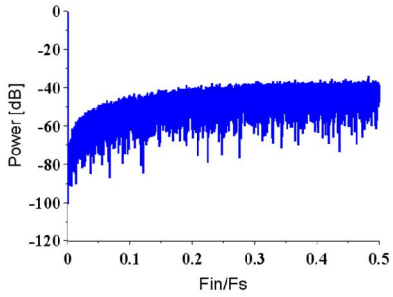


Fig. 2. Power spectrum of the LP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: Fin/Fs = 1/16,384)

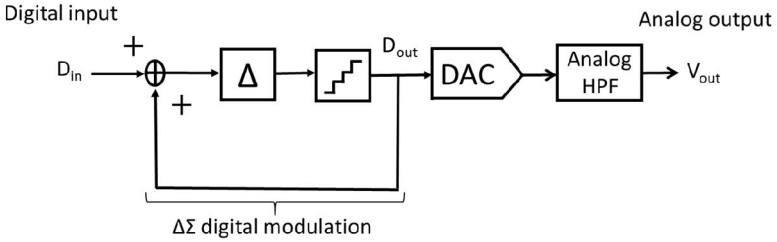


Fig. 3. Block diagram of the first-order HP ΔΣ DA converter.

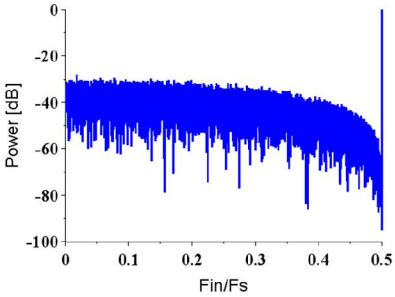
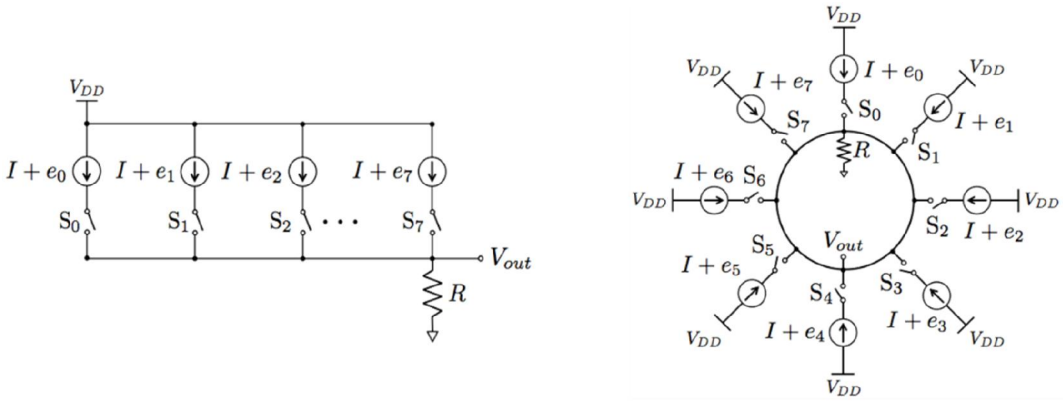


Fig. 4. Power spectrum of the HP ΔΣ modulator output.
(Input sine wave amplitude: 1, normalized frequency: Fin/Fs = 8191/16384)

3. Multi-bit ΔΣ DA modulator with binary unit cells

3.1 Binary unit current cell mismatches of segmented DAC

We assume that a DAC which follows the modulator has 9-level resolution; its digital input takes the values of 0, 1, 2, ..., 6, 7, or 8 (Fig. 5). Though ideally all currents should be equal, in reality they can be slightly different due to such as process variation inside an IC chip. e_k in Fig. 5 indicates current mismatch component of I_k. In the case of Fig. 5(a), the mismatch effects cause almost flat power spectrum in the entire band as well as harmonic distortions.



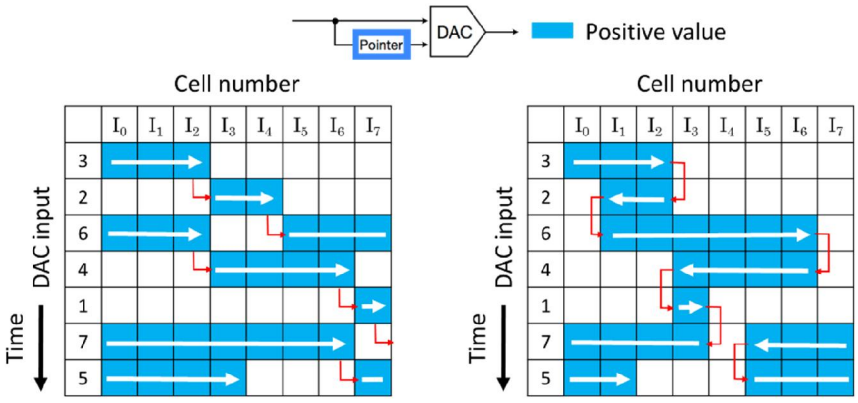
(a) An 8-unit segmented current steering DAC. (b) Its ring configuration.

Fig. 5. Current DAC in the case of the binary.

3.2 DWA algorithm for binary

Now let us consider to use a DWA DAC (Fig. 5(b)) for linearity improvement [3, 6, 9, 10, 11,12]. The DWA DAC storing the next-cell-selection position with a pointer P(n) controls the cell selection in a rotation manner, which leads to nonlinearity errors of the multi-bit DAC to be noise-shaped. (Averaged error around DC is zero.) Fig. 6 shows unit-current-cells of ON when its input data is 3, 2, 6…. In the case of DWA type I as shown in Fig. 6(a), first, current cells (0, 1, 2) are selected when the digital input data is 3. Next, current cells (3, 4) are selected when the digital input data is 2. On the other hand, in the case of DWA type II in Fig. 6(b), first, current cells (0, 1, 2) are selected when the digital input data is 3. Next, current cells (2, 1) are selected when the digital input data is 2.

In the case of the binary, the methods with DWA type I and DWA type II are effective for LP and HP ΔΣ modulators respectively [3-7].



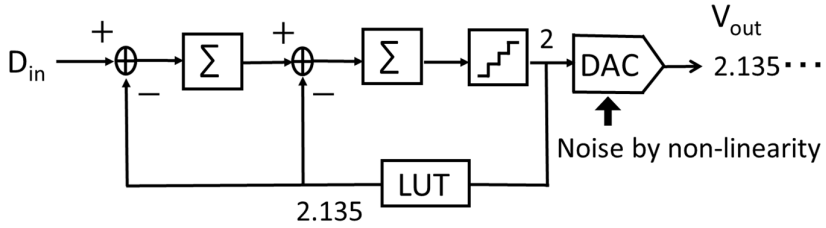
(a) DWA type I (b) DWA type II

Fig. 6. Selection method of current cells with DWA in the case of the binary.

3.3 Self-calibration

In Fig. 7, DAC analog output is 2.135.. due to nonlinearity of the multi-bit DAC when the modulator output is 2. Self-calibration uses this value of '2.135', which is fed-back to the digital input [5]. We use Look Up Table (LUT) in order to realize the self-calibration. The LUT data are created to measure the feedback values with a high linear and high resolution ADC in advance, and the LUT output data are selected corresponding to the LUT input. It is not necessary to calculate data every time, so a processor is able to reduce calculation load and efficiently execute processing. Note that if the data bit length in the LUT is larger (i.e. a larger size LUT and a high resolution ADC are used), more accurate self-calibration can be performed.

For example, suppose that digital output for D_{out} is 2 and the DAC output is 2.135 due to their nonlinearity in Fig. 7. Then the digital values of 2.135 (rounded digital) obtained from LUTs are fed-back to the input.



	LUT input	LUT output
DAC		
LUT	2	2.135

Fig. 7. Circuit with LUT block.

3.4 SNDR evolution

Signal to Noise and Distortion Ratio (SNDR) is one of the DAC performance indices; it is the ratio of the signal component power to the generated noise power. The DAC performance becomes better as its SNDR is improved.

3.5 Simulation results for binary

3.5.1 Linearity improvement of LP model circuit

The previous sections have investigated the techniques using DWA type I and self-calibration algorithm. DWA type I is effective for LP model in the case of the binary [3, 6, 9, 10, 11,12]. We compare 4 circuits (the conventional circuit, DWA, self-calibration and its combination) as shown in Table 1, and verify the linearity improvement. Fig. 8 shows LP④ circuits. They are different from DWA type I, self-calibration and its combination. We use a sinusoidal signal input (D_{in}) whose period is 14K-point and its amplitude is 3.5 and center value is 4.0. Unit-current-cells have some errors.

Fig. 9 shows power spectrums for circuits LP① to LP④. Table 2 shows mismatch e_k for Fig. 9. LP ④ in Fig. 9 indicates that noise of the low frequency band is reduced. The circuits of Fig. 9 LP⑤, LP ⑥ use DWA type II, and we have confirmed that the noise power near signal band is estimated by DWA type II.

Fig. 10 shows SNDR comparison; mismatch standard deviation (σ) is varied. SNDRs are averaged values among 5 sets (σ = 5.0%, 0.05%) and 10 sets (σ = 1.0%, 0.1%) of the unit-current-cells. Note that realistic mismatch standard deviation σ by process variation is 0.5 to 1.0 % with relatively large size MOSFET while it can be 2-5% if very small size MOSFET. We see that the SNDR values of the proposed circuit LP④ is higher than other circuit LP① to LP③. SNDR values of the LP① to LP④ are improved in Fig. 10(d) because the mismatch is relatively small; its state is close to ideal.

Note that self-calibration itself can improve the overall linearity though the feedback digital values in LUT are truncated. Then, using DWA together can further diffuse the errors which cannot be corrected only with self-calibration.

Table 1. Simulation circuits of LP① to LP④.

	DWA type Ⅰ	Self-calibration
LP①	×	×
LP②	○	×
LP③	×	○
LP④	○	○

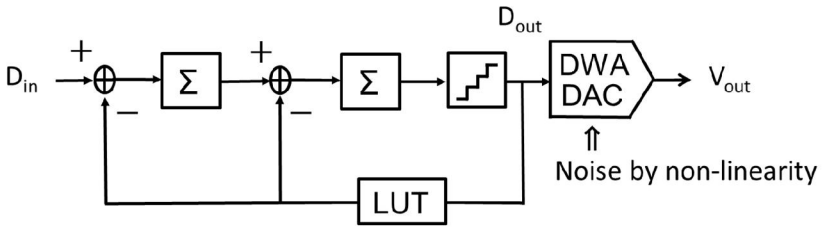
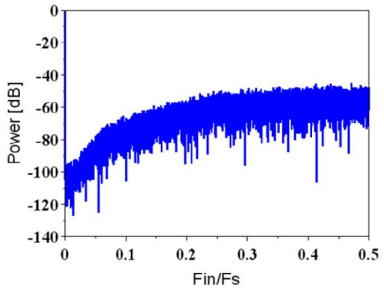
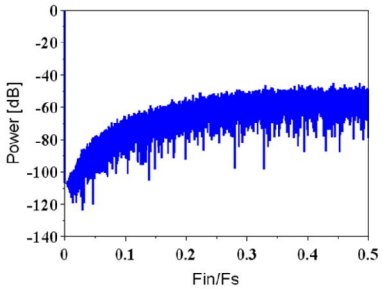


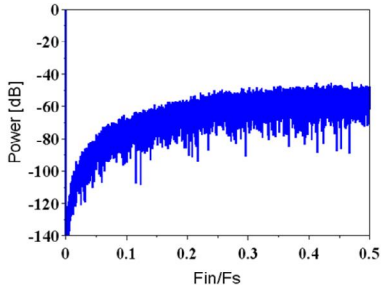
Fig. 8. Proposed LP model circuit with DWA DAC and LUT for self-calibration.



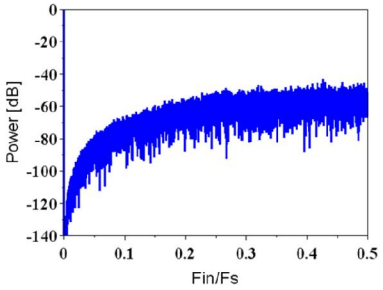
LP① w/o DWA type Ⅰ nor self-calibration



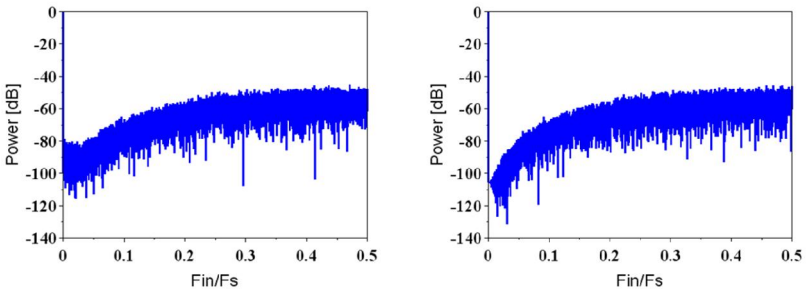
LP② w/ DWA type Ⅰ, w/o self-calibration



LP③ w/o DWA type Ⅰ, w/ self-calibration

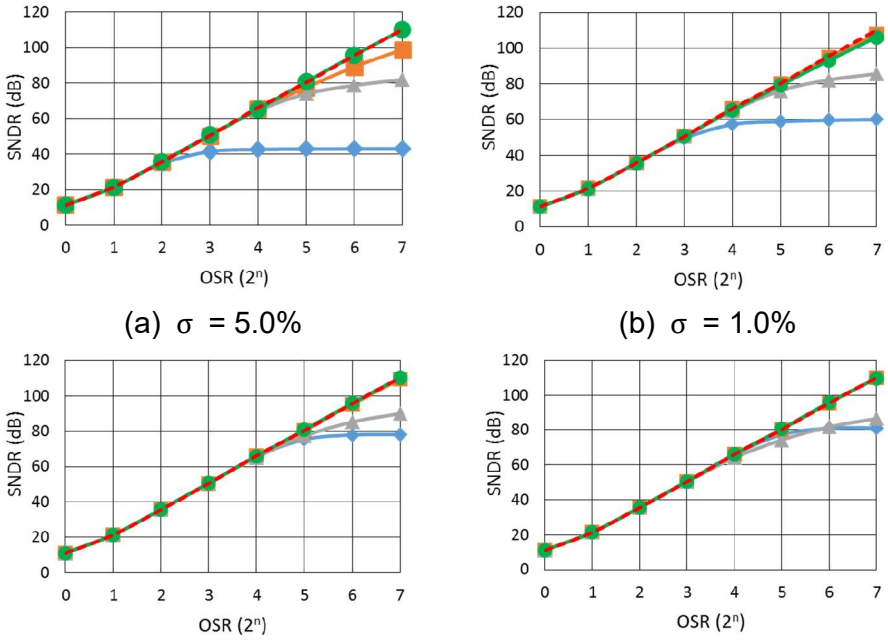


LP④ w/ DWA type Ⅰ & self-calibration



LP⑤ w/ DWA type Ⅱ , w/o self-calibration　　LP⑥ w/ DWA type Ⅱ & self-calibration

Fig. 9. Power spectrum of binary LP model circuits (σ = 1.0%) (Fin/Fs = 1/16384).



(a) σ = 5.0%　　(b) σ = 1.0%

(c) σ = 0.1%　　(d) σ = 0.05%

Fig. 10. SNDR comparison of binary LP model.

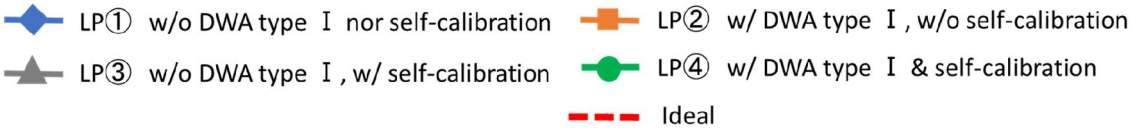


Table 2. Values for mismatch e_k.

Mismatch : e_k	Standard deviation : σ = 1%
e_0	-0.00240643411874771
e_1	-0.01858388085849580
e_2	0.01043109801442670
e_3	0.00512259645232309
e_4	0.00896906661801040
e_5	-0.00481840183704237
e_6	-0.00724947011098265
e_7	0.00853542584050834

3.5.2 Linearity improvement of HP model circuit

Similarly, we have verified the effectiveness of DWA type II and self-calibration. DWA type II is effective for HP model in the case of the binary [3-7]. We compare 4 circuits (Table 3). Fig. 11 shows HP④ circuits. We use a sinusoidal signal input (D_{in}) whose period is 14K-point and its amplitude is 3.5 and the center value is 4.0. Unit-current-cells have some errors.

Fig. 12 shows power spectrums for circuits HP① to HP④ with mismatch e_k of the Table 2. HP④ in Fig. 12 indicates that noise of the high frequency band is reduced. The circuits of Fig. 12 HP⑤, HP ⑥ use DWA type I represents that the noise power near signal band is estimated by DWA type I.

Fig. 13 shows SNDR comparison, and we see that the SNDR values of the proposed circuit HP④ is higher than other circuit HP① to HP③ in all mismatch standard deviations.

Like LP circuits, the self-calibration itself can improve the overall linearity though the feedback digital values in LUT are truncated. Then, using DWA together can further diffuse the errors which cannot be corrected only with self-calibration.

Table 3. Simulation circuits of HP① to HP④.

	DWA type Ⅱ	Self-calibration
HP①	×	×
HP②	○	×
HP③	×	○
HP④	○	○

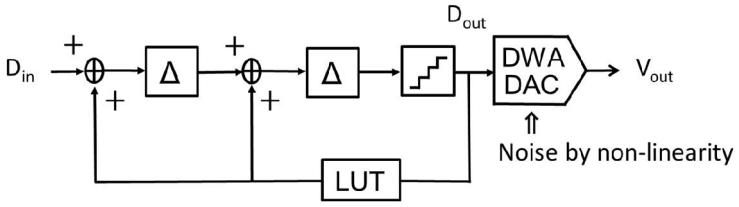
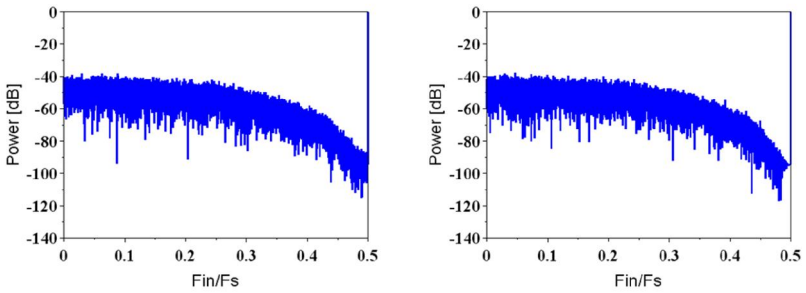
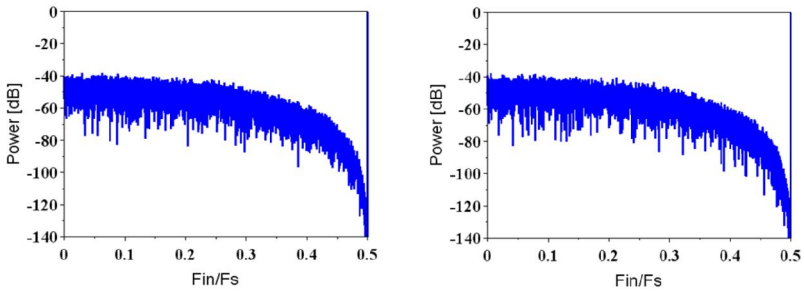


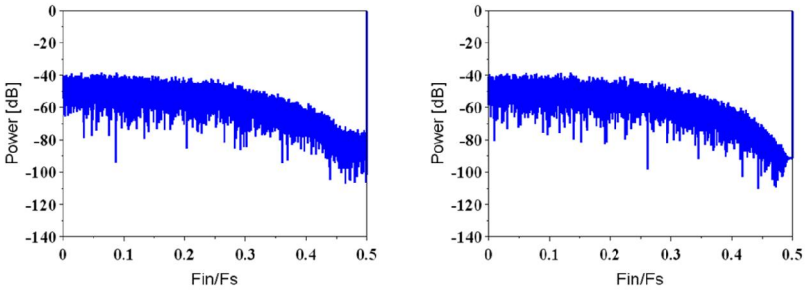
Fig. 11. Proposed HP model circuit with DWA DAC and LUT for self-calibration.



HP① w/o DWA type Ⅱ nor self-calibration HP② w/ DWA type Ⅱ , w/o self-calibration

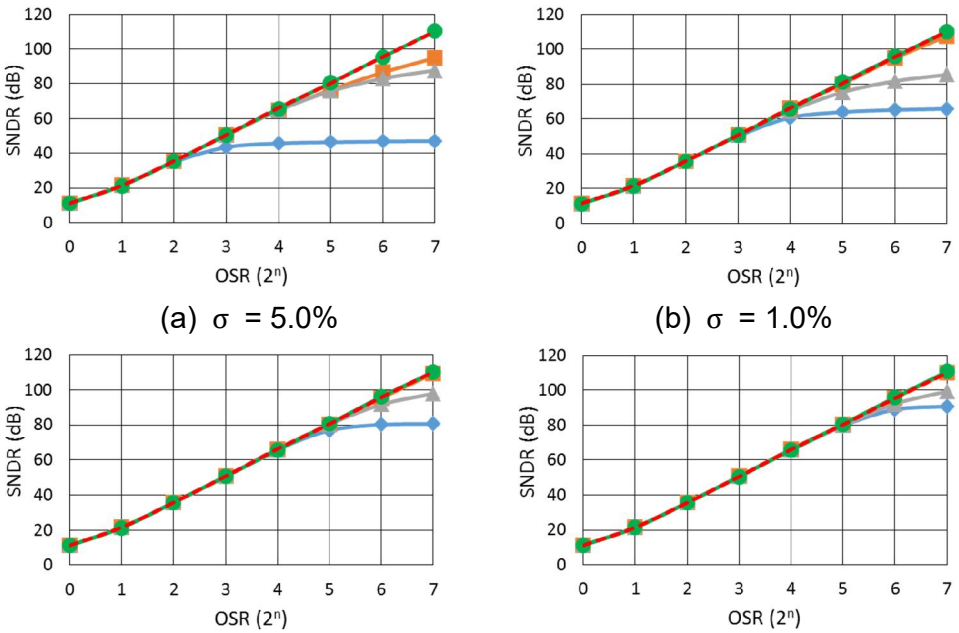


HP③ w/o DWA type Ⅱ , w/ self-calibration　　HP④ w/ DWA type Ⅱ & self-calibration



HP⑤ w/ DWA type Ⅰ , w/o self-calibration　　HP⑥ w/ DWA type Ⅰ & self-calibration

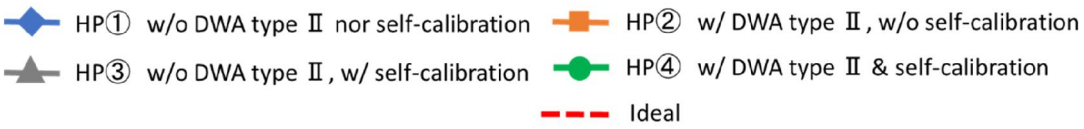
Fig. 12. Power spectrum of binary HP model circuits (σ = 1.0%) (Fin/Fs = 8191/16384).



(a) σ = 5.0%　　(b) σ = 1.0%

(c) σ = 0.1%　　(d) σ = 0.05%

Fig. 13. SNDR comparison of binary HP model.

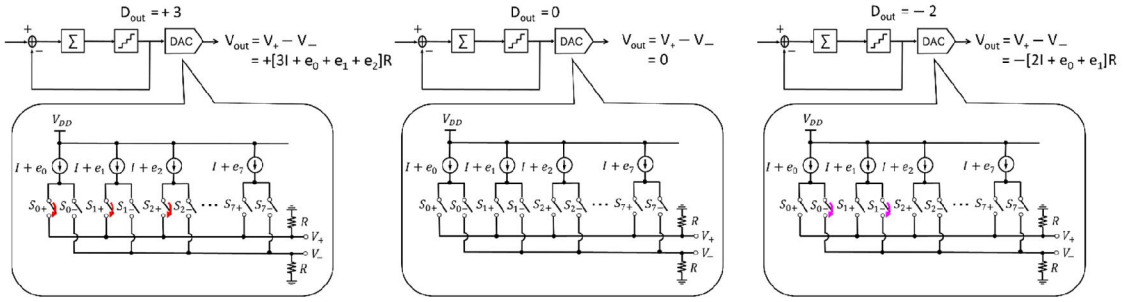


4. Multi-bit ΔΣ DA modulator with ternary unit cells

4.1 Ternary unit current cell mismatches of segmented DAC

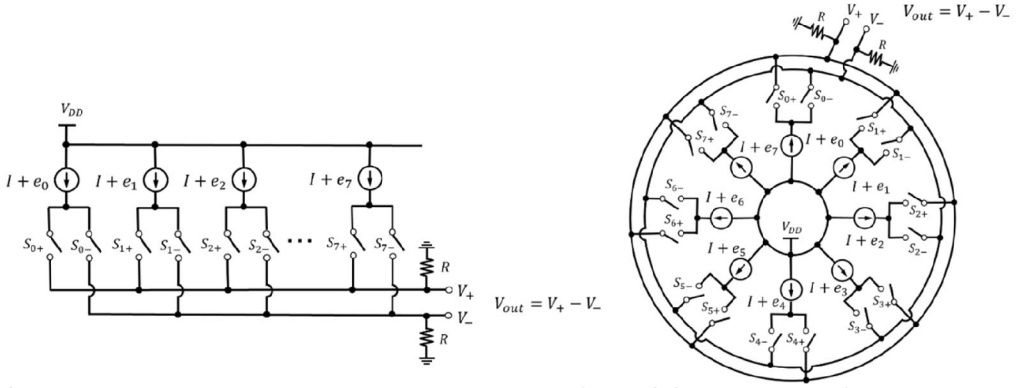
We consider the ternary value case (positive, zero, negative) (Fig. 14) [13, 14]. V_{out} is obtained from difference between V_+ and V_-. For example, V_{out} is a positive voltage when D_{out} is +3 (Fig. 14(a)). In contrast, V_{out} is a negative voltage when D_{out} is -2 (Fig. 14(c)). Of course, V_{out} is 0 when D_{out} is 0 (Fig. 14(b)). On the other hand, in the conventional binary digital, they are positive or zero.

We assume that a DAC which follows the modulator has 17-level resolution; its digital input takes the values of -8, -7, … 0, +1, +2, ..., +6, +7, or +8 (Fig. 15). As described in section 3.1, all currents can be slightly different due to such as process variation inside an IC chip. So, in case of Fig. 15(a), the mismatch e_k effects cause almost flat power spectrum in the entire band as well as harmonic distortions.



(a) V_{out} is positive. (b) V_{out} is zero. (c) V_{out} is negative.

Fig. 14. Digital value cases; positive, zero, negative.



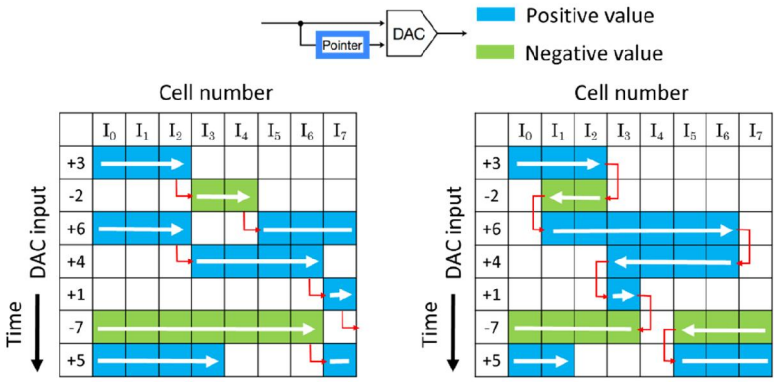
(a) An 8-unit segmented current steering DAC. (b) Its ring configuration.

Fig. 15. Current DAC in the case of ternary.

4.2 DWA algorithm for ternary

We consider a DWA DAC storing the position with a pointer P(n) of the ternary (Fig. 15(b)) [14]. Fig. 16 shows unit-current-cells of ON when the input data is +3, -2, +6…. On the one hand, in the case of DWA type I in Fig. 16(a), first, current cells (0, 1, 2) are selected when the digital input data is +3. Next, current cells (3, 4) are selected when the digital input data is -2. On the other hand, in the case of DWA type II in Fig. 16 (b), first, current cells (0, 1, 2) are selected when the digital input data is +3. Next, current cells (2, 1) are selected when the digital input data is -2.

Here, we have newly found that the DWA type I is effective for LP and HP model in the case of the ternary, so simulated using DWA type I for LP and HP circuits. On the other hand, DWA type I is effective for LP, and DWA type II is effective for HP in the case of the binary. Table 4 shows effective DWA type for binary and ternary cases.



(a) DWA type Ⅰ (b) DWA type Ⅱ

Fig. 16. Selection method of current cells with DWA in the case of the ternary.

Table 4. Effective DWA type for binary and ternary cases.

	LP	HP
Binary (+, 0)	Type Ⅰ	Type Ⅱ
Ternary (+, 0, −)	Type Ⅰ	Type Ⅰ

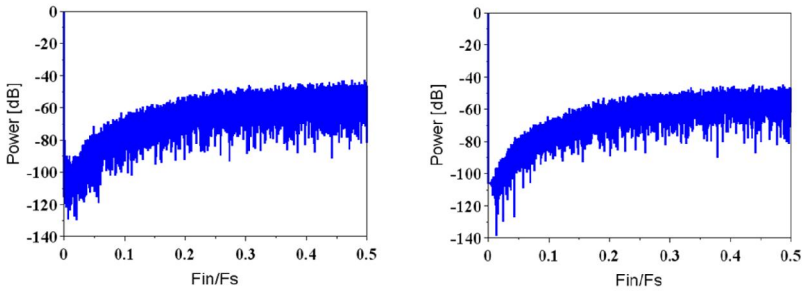
4.3 Simulation results for ternary

4.3.1 Linearity improvement of LP model circuit

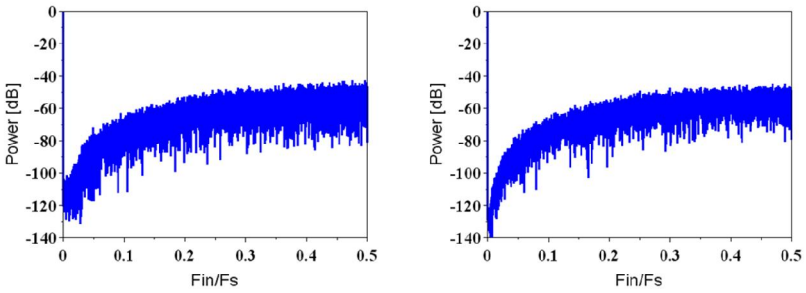
We have confirmed the techniques of DWA type I and self-calibration algorithms using simulation. DWA type I is effective for LP model in the case of the ternary. As the same as in section 3.5.1, we have compared 4 circuits in Table 1 and Fig. 8, and verified the linearity improvement. We use a sinusoidal signal input (D_{in}) with its period of 14K-point, amplitude of 7.5 and center value of 0.0. Also unit-current-cells have some errors.

Fig. 17 shows power spectrums for circuits LP① to LP④. Fig. 17 LP④ indicates that the noise is reduced in the low frequency region. The circuits of Fig. 17 LP⑤, LP⑥ use DWA type II, and the noise power near the signal band is increased by DWA type II.

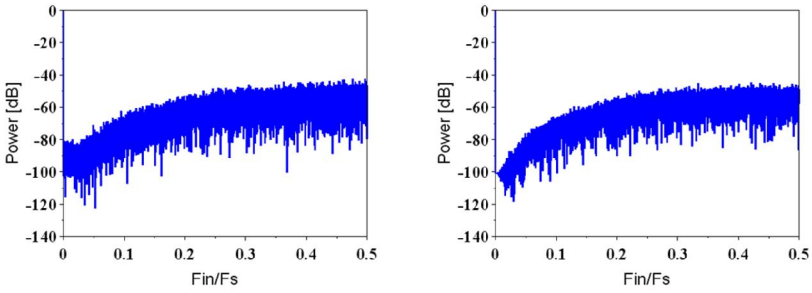
Fig. 18 shows SNDR comparison. SNDRs are averaged values among 5 sets (σ = 5%, 0.05%) and 10 sets (σ = 1.0%, 0.1%) of the unit-current-cells. We see from Fig. 18 that SNDR values of the LP④ is higher than other circuit LP① to LP③. The reason is that using DWA and self-calibration as with section 3.5. In addition, the number of DAC output levels in the case of the ternary is larger than that of the binary; ternary output level is 17 whereas binary output level is 9. The larger the number of the output level is, the more effective the proposed method is.



LP① w/o DWA type Ⅰ nor self-calibration LP② w/ DWA type Ⅰ, w/o self-calibration

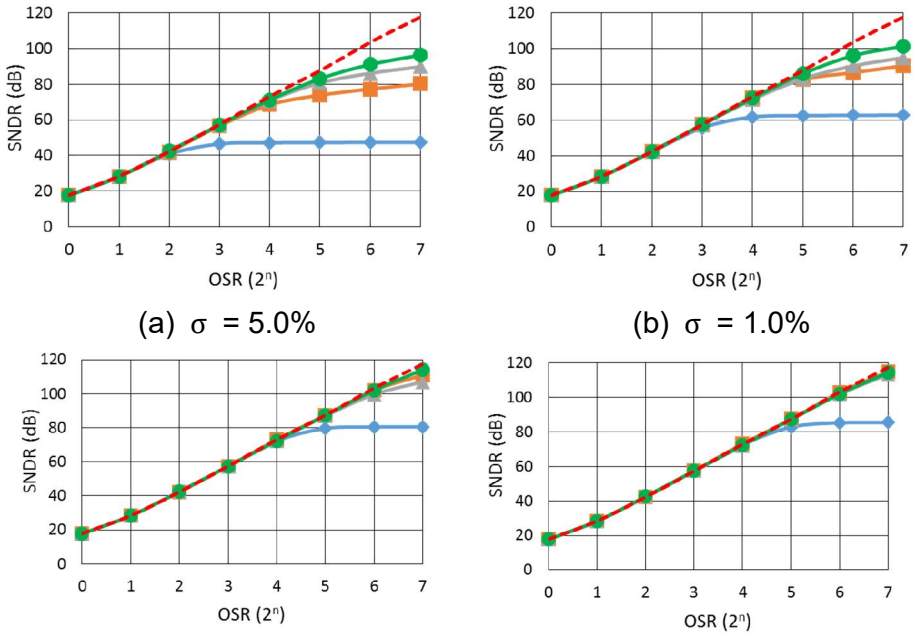


LP③ w/o DWA type Ⅰ, w/ self-calibration　　LP④ w/ DWA type Ⅰ & self-calibration



LP⑤ w/ DWA type Ⅱ, w/o self-calibration　　LP⑥ w/ DWA type Ⅱ & self-calibration

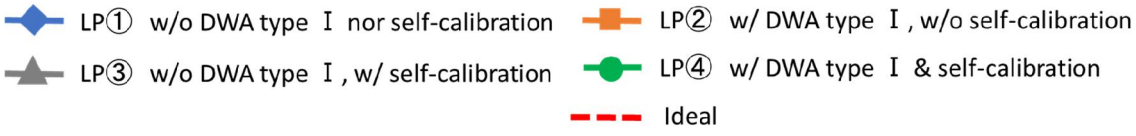
Fig. 17. Power spectrum of ternary LP model circuits (σ = 1.0%) (Fin/Fs = 1/16384).



(a) σ = 5.0%　　(b) σ = 1.0%

(c) σ = 0.1%　　(d) σ = 0.05%

Fig. 18. SNDR comparison of ternary LP model.

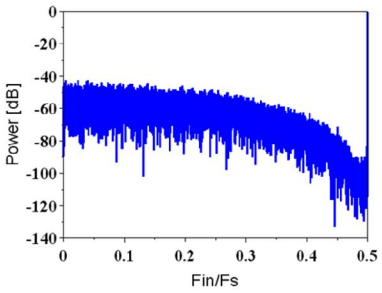


4.3.2 Linearity improvement of HP model circuit

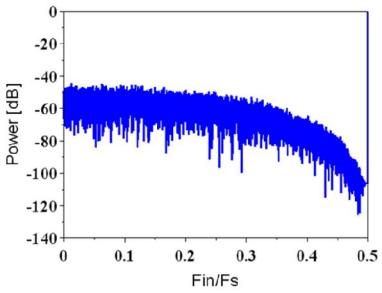
In a similar manner, we have simulated 4 circuits in the Table 3 and Fig. 11. DWA type I is effective for HP model in the case of the ternary, whereas DWA type II is not. We use a sinusoidal signal input (D_{in}) with the period of 14K-point, amplitude of 7.5 and center value of 0.0. Unit-current-cells have some errors.

Fig. 19 shows power spectrums. Fig. 19 HP④ represents that noise is reduced in the high frequency region. On the other hand, the circuits of Fig. 19 HP⑤, HP⑥ use DWA type II, and the noise near signal band is increased by DWA type II. Fig. 20 shows SNDR comparison. SNDRs are averaged values among 5 sets (σ = 5%, 0.05%) and 10 sets (σ = 1.0%, 0.1%) of the unit-current-cells. We see that SNDR values of the HP④ is the most improved in Fig. 20.

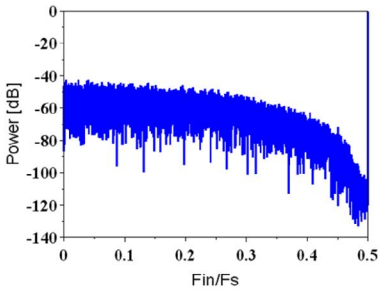
In this research, we have newly found the effectiveness of using DWA type I and the ineffectiveness of using DWA type II for HP model in the case of the ternary (Table 4). In the case of DWA type I, all currents (I_0 to I_7) are equally selected. Accumulated mismatches e_k are time-averaged to zero, so the noise is reduced in the low frequency band. In contrast, in the case of the ternary, the DAC outputs of the plus and minus are accumulated, and the noise is reduced in the high frequency. On the other hand, DWA type II selects the currents alternately for going forwards and back, and this selection decreases noise in the high frequency band. In the case of the binary, the DAC outputs of only the plus is used, and then DWA type II is effective in the high frequency.



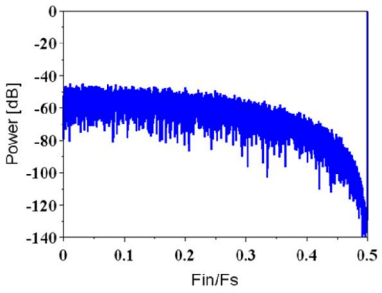
HP① w/o DWA type Ⅰ nor self-calibration



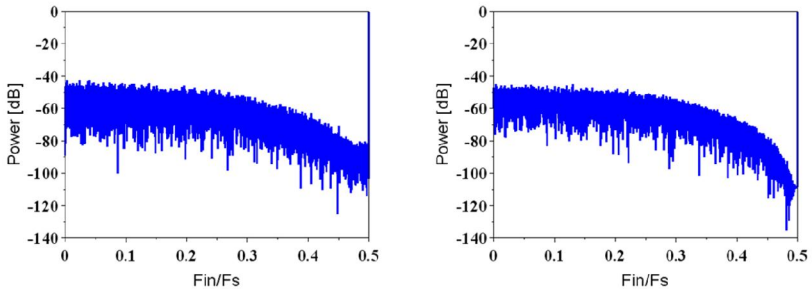
HP② w/ DWA type Ⅰ, w/o self-calibration



HP③ w/o DWA type Ⅰ, w/ self-calibration

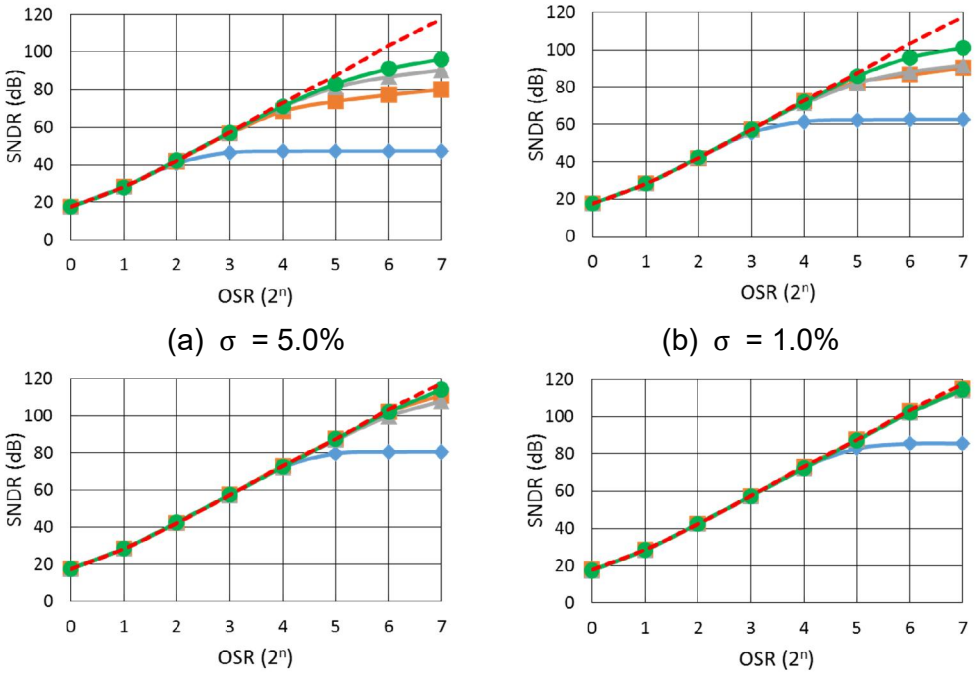


HP④ w/ DWA type Ⅰ & self-calibration



HP⑤ w/ DWA type Ⅱ , w/o self-calibration　　HP⑥ w/ DWA type Ⅱ & self-calibration

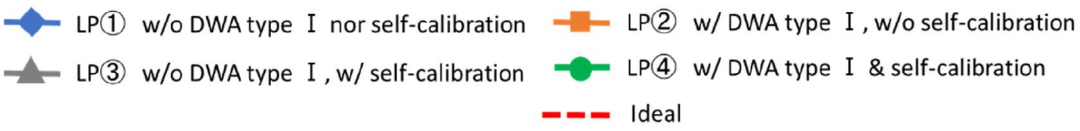
Fig. 19. Power spectrum of ternary HP model circuits (σ = 1.0%) (Fin/Fs = 8191/16384).



(a) σ = 5.0%　　(b) σ = 1.0%

(c) σ = 0.1%　　(d) σ = 0.05%

Fig. 20. SNDR comparison of ternary HP model.



5. Conclusion

We have investigated digital techniques for linearity improvement in multi-bit ΔΣ DA converters for three values digital; values are positive, zero, negative. We have derived DWA and self-calibration algorithms, as well as their combination, and validated their effectiveness with MATLAB simulation. The proposed circuits for both LP and HP model using DWA and self-calibration can achieve higher SNDR values than the conventional. When the mismatches of the DWA are relatively large, the proposed method is effective. In addition, we have found and verified that DWA type I is effective for HP model in the case of the ternary although DWA type II is effective for HP model in the case of the binary. The proposed systems consist of mostly digital and they can be easily implemented.

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